UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/525,139	02/16/2005	Emmanuel Ardichvili	FR02 0087	1770

25235 7590 06/10/2009

HOGAN & HARTSON LLP
ONE TABOR CENTER, SUITE 1500
1200 SEVENTEENTH ST
DENVER, CO 80202

EXAMINER	
FOTAKIS, ARISTOCRATIS	
ART UNIT	PAPER NUMBER
2611	

NOTIFICATION DATE	DELIVERY MODE
06/10/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentcolorado@hhlaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/525,139	ARDICHVILI ET AL.	
	Examiner	Art Unit	
	ARISTOCRATIS FOTAKIS	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04/24/2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 24, 2009 has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1 – 2, 4 – 5, 7, 10 and 12 – 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harju et al ("*A Flexible Rake Receiver Architecture for WCDMA Mobile Terminals*" Digital and Computer Systems Laboratory, Tampere University of Technology, Tampere, Finland, March 20 – 23, 2001) in view of Medlock et al (US 2002/0037027).

Re claims 1, 12 and 13, Harju teaches of a receiver for receiving an input signal comprising a series of samples, said receiver comprising one delay line (circular buffer, conclusions, Figs. 2 and 3), characterized in that the delay line is configured to delay said input signal by a series of delays and is divided into a series of delay sub-lines (*It is inherent that a circular buffer includes a delay line that is divided in a series of*

delay taps or memory locations or memory address) each being used to write one from the series of samples of said input signal, each of the delay sub-lines including a memory area to receive at least one sample from the series of samples (memory address, highlighted in Fig.3, Page 10), and in that the solution further comprises control means configured to generate read addresses (read I/Q samples, Fig.3) of the samples in the delay sub-lines from the series of samples of the input signal, so that a read address is equal to a difference between a write address of a sample in a delay sub-line of the input signal (circular address generator. Fig. 3) and a delay expressed as a number of sampling periods from the series of delays (offset address registers, Fig. 3, Page 10). However, Harju does not specifically teach of wherein the delay line is directly coupled to a plurality of multiplexers for providinq early, in-time, and late outputs.

Medlock teaches of each memory block 902 (Fig.9) in the memory 304 (Fig.6) is further divided into segments 1002a-1002h (Fig.10). Each memory segment 1002 is coupled to a separate bussing element 1004a-1004h via multiple signal lines 1006a-1006h (Fig.10). In general, each signal line 1006 carries an I and Q data pair onto the bussing element 1004. Each bussing element 1004 sequentially reads out data from its respective segment 1002. Multiple despreading circuits 600a-600b are connected to the memory segments 1002 via a bus 1010. Each despreading circuit 600 includes a selector circuit 602 and a rake finger 1008. The selector circuit 602 includes a block multiplexer 1012, three sample multiplexers 1014a-1014c, and a cache 1016. The rake finger 1008 includes hardware known in the art. The block multiplexer 1012 selects one

of the bussing elements 1004 to read data from one of the segments 1002. The sample multiplexers 1014 selects the Early, On-time, and Late samples among the I and Q data pairs read from a segment 1002, which was selected by the block multiplexer 1012. The I and Q data pairs selected by the sample multiplexers 1014 are stored into the cache 1016 to be processed by the rake finger 1008 (Fig.10 and Paragraphs 0063 - 0064).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the delay line directly coupled to a plurality of multiplexers (1012 and 1014a-c, Fig.10) for providinq early, in-time, and late outputs to have them processed by the rake finger.

Re claim 2, Harju teaches of the delay line comprising a single series of delay sub-lines (*It is inherent that a delay buffer includes a delay line that is divided in at least a series of delay taps or memory locations or memory address*) (Fig. 3).

Re claim 3, Harju teaches all the limitations of claim 1 except of the delay line comprising various series of delay sub-lines.

Medlock teaches of a circular buffer comprising a set of registers. Once data has been stored into memory, a despreading circuit (e.g., a rake receiver), which includes multiple rake fingers, can access the data. The multiple rake fingers can substantially simultaneously access data in the memory via a selector circuit for each rake finger. Each selector circuit includes multiple multiplexers controlled by a set of select lines. The select lines are controlled by an external controller (Paragraph 0025, Fig.10).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have the delay line comprising various series of delay sub-lines to achieve faster processing.

Re claim 4, Harju teaches of a delay sub-line is accessible with a frequency twice as fast as the samples of an input signal received by the receiver (equation 2, Page 11).

Re claim 5, Harju teaches of wherein one memory area is associated to one delay sub-line (memory address with an offset, Fig.3).

Re claim 6, Harju teaches all the limitations of claim 1 except of that the samples of a series of samples are accessible in parallel in the write mode or read mode in the delay sub-lines. Medlock teaches of the samples of a series of samples are accessible in parallel in the write mode or read mode in the delay sub-lines (Fig.10, 1014a – 1014c).

Re claim 7, Harju teaches of the read addresses of the samples of a series of samples are situated at addresses immediately adjacent or equal to one another (Fig.3).

Re claim 8, Harju teaches all the limitations of claim 3 except of two series of samples are read in parallel. Medlock teaches of two series of samples are read in parallel (Fig.9, Paragraphs 0061 - 0063).

Re claim 9, Harju and Medlock teach all the limitations of claim 8 as well as Medlock teaches of wherein the delay line comprises selection means of a series of delay sub-lines to which belongs one of the two series of samples read as a function of the delay (#1012, Fig.10).

Re claim 10, Harju teaches of the delay line comprises a position factor (cursor, Fig.3) indicating the position of a reference sample from a series of samples of an input signal in the series of delay sub-lines to which it belongs (Page 10, Fig.3).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harju and Medlock in view of Kim et al (US 6,788,731).

Harju and Medlock teach all the limitations of claim8 as well as Medlock teaches of the memory areas for a series of samples read (FIFO cache, Paragraph 0064) which correspond to a first and second series of delay sub-lines (Fig.10). However, Harju and Medlock do not specifically teach of that the memory areas are regrouped into a first and a second group, the first group regrouping a current series of current areas and a next series of areas which can each correspond to the first series of delay sub-lines and the second group regrouping the current series of areas and the next series of areas which can each correspond to the second series of the delay sub-

lines, so that the memory areas for a series of samples read are identical for each equal position factor value.

Kim teaches of that the memory areas are regrouped into a first and a second group (BANK 0 and BANK 1, Figs.6 - 7), the first group (BANK 0) regrouping a current series of current areas (0 – 7, Fig.7) and a next series of areas (16 – 23, Fig.7) and the second group (BANK 1) regrouping the current series of areas (8 – 15, Fig.7) and the next series of areas (24 – 31, Fig.7), so that the memory areas for a series of samples read are identical for each equal position factor value (#306, Fig.9).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have regrouped into two groups the samples from the delay lines in the FIFO cache of Medlock so as to increase and reduce processing time of the system.

Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harju in view of Medlock and further in view of Kim et al (US 6,788,731).

Harju, Medlock and Kim teach of a receiver for receiving an input signal comprising a series of samples, said receiver comprising one delay line, characterized in that the delay line is configured to delay said input signal by a series of delays and is divided into a series of delay sub-lines each being used to write one from the series of samples of said input signal, each of the delay sub-lines including a memory area to receive at least one sample from the series of samples, and further comprises control

means configured to generate read addresses of the samples in the delay sub-lines from the series of samples of the input signal, so that a read address is equal to a difference between a write address of a sample in a delay sub-line of the input signal and a delay expressed as a number of sampling periods from the series of delays, wherein the delay line comprises various series of delay sub-lines, two series of samples are read in parallel, and the memory areas are regrouped into a first and a second group, the first group regrouping a current series of current areas and a next series of areas which can each correspond to the first series of delay sub-lines and the second group regrouping the current series of areas and the next series of areas which can each correspond to the second series of the delay sub-lines, so that the memory areas for a series of samples read are identical for each equal position factor value (see claims 1 and 11).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ARISTOCRATIS FOTAKIS whose telephone number is (571)270-1206. The examiner can normally be reached on Monday - Thursday 6:30 - 4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Aristocratis Fotakis/

Examiner, Art Unit 2611

/Chieh M Fan/

Supervisory Patent Examiner, Art Unit 2611